Patent
Attorney's Docket No. 019519-192

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



In re Patent Application of )
Shinichi TAKAGI et al. ) Group Art Unit: 2815
Application No.: 09/138,582 ) Examiner: S. Clark
Filed: August 24, 1998 )
For: SEMICONDUCTOR ELEMENT MODULE AND SEMICONDUCTOR DEVICE WHICH PREVENTS SHORT CIRCUITING (As Amended) )

#5/a
6/16/99
V. Vannall



**AMENDMENT**

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated March 18, 1999, kindly amend the above-identified application as follows.

**IN THE TITLE**:

Kindly amend the title to read: --SEMICONDUCTOR ELEMENT MODULE AND SEMICONDUCTOR DEVICE WHICH PREVENTS SHORT CIRCUITING--.

**IN THE CLAIMS**:

Please amend claims 1-8 as follows.

1. (Amended) A semiconductor element module, comprising:

a package[,];

a semiconductor element arranged [on] within said package; and

a plurality of leads provided on sides of the package [so that an opening] with an open end of each of said leads [is oriented to the side of] extending at least to a package attaching plane, the plurality of leads being electrically connected through said package to said semiconductor element and serving to connect said semiconductor element to an external circuit;

wherein a shape of the package provides a level [differences] difference between said package and the plurality of leads proximate [is provided on the side of] said package attaching plane [of each of package sides] so that a space is formed from each of said plurality of leads and the package; and

a substance having conductor patterns for lead connection on a mounting plane thereof wherein each of said leads is soldered to the substrate through holes in each of said conductor patterns so that the bottom of said package forms a prescribed space from the mounting plane.

4. (Amended) A semiconductor element module, comprising:

a package[,];

a semiconductor element arranged [on] within said package;

a plurality of leads provided on sides of the package [so that an opening] with an open end of each of said leads [is oriented to the side of] extending at least to a package attaching plane, the plurality of leads being electrically connected through said

package to said semiconductor element and serving to connect said semiconductor element to an external circuit; and

brazing [materials each] material for connecting said package and each of said leads [, wherein said level difference forms a space permitting each said leads to be shaped at it portion near to said package];

wherein a shape of the package provides a level [differences] difference between said package and the plurality of leads proximate [is provided on the side of] said package attaching plane [of each of package sides] so that a space is formed from each of said plurality of leads and the package; and

wherein said level difference permits each of said leads to be shaped proximate said package.

5. (Amended) A semiconductor element module, comprising:

a package; [and]

a semiconductor element arranged [on] within said package; and

a plurality of leads provided on sides of the package [so that an opening] with an open terminal of each of said leads [is oriented to the side of] extending at least to a package attaching plane, the plurality of leads being electrically connected through said package to said semiconductor element and serving to connect said semiconductor element to an external circuit;

wherein a shape of said leads provides a level difference [is provided at a portion of each said leads not connected to said package so that the] between said package

package and the plurality of leads proximate said package attaching plane, said shape being such that a width of each of said leads on the side where the lead and the package are connected is thick and that on [the] a side of its [opening] open end is thin; and

a substrate having conductor patterns for lead connection on a mounting plane thereof wherein each of said leads is soldered to the substrate through holes in each of said conductor patterns so that the bottom of said package forms a prescribed space from the mounting plane; and

wherein said level difference serves to prevent short-circuiting between the leads adjacent to each other.

8. (Amended) A semiconductor element module comprising:

a package;

a semiconductor element arranged [on] within said package;

a plurality of leads provided on sides of the package [so that an opening] with an open terminal of each of said leads [is oriented to the side of] extending at least to a package attaching plane, the plurality of leads being electrically connected through said package to said semiconductor element and serving to connect said semiconductor element to an external circuit;

brazing [materials] material for connecting said package and each of said leads[, wherein said level difference provides different mechanical strengths permitting each said leads to be shaped at its portion near to said package];

wherein a shape of said leads provides a level difference [is provided at a portion of each said leads not connected to said package so that the] between said package and the plurality of leads proximate said package attaching plane, said shape being such that a width of each of said leads on the side where the lead and the package are connected is thick and that on [the] a side of its [opening] open end is thin; and

wherein said level difference provides different mechanical strengths permitting each of said leads to be bent proximate said package.

A' Cmd'd

REMARKS

Claims 1-10 are presently pending. The amendments to claims 1-6 and 8 are intended only to clarify the claims, and it is submitted do not change the scope of the claimed invention.

The Office Action objects to the title. In response, Applicants have amended the title to be more descriptive of the invention to which the claims are directed.

The Office Action objects to Figures 7, 8 and 9, stating that they should be labeled "Prior Art." In response, Applicants provide a Request for Approval of Drawing Changes and copies of Figures 7, 8 and 9 with changes in red ink addressing this objection.

The Office Action rejects claim 4 under 35 U.S.C. §112, second paragraph, as being indefinite because "level difference" has no antecedent. In response, Applicants have amended claim 4 to address this concern.

The Office Action rejects claims 1 and 9 under 35 U.S.C. §103(a) over Japanese Patent 1-39051 (Hirata '051). Applicants respectfully traverse this rejection.

The present invention concerns a semiconductor apparatus configured to prevent solder short circuiting while maintaining the structural integrity and dimensional tolerances of the semiconductor apparatus. Solder short circuiting is a problem which occurs when capillary attraction causes molten solder to improperly flow into the slight gap between a semiconductor apparatus package and the substrate to which it is being soldered.

One way of avoiding solder short circuiting is by simply raising the entire semiconductor package bottom away from the substrate as it is being soldered. A sufficient clearance between the package and the substrate prevents capillary attraction from drawing the solder beyond where the solder is desired. However, the method of raising the package from the substrate suffers from several drawbacks. The most obvious drawback is that the increased height of the finished assembly requires more physical space in the finished assembly. Another drawback is that a raised configuration weakens the connecting strength between the package and the substrate. In addition, it can be difficult to ensure a level fit between the package and the substrate while the package is being soldered in a raised position. Another significant drawback occurs because impurities may accrue beneath a package raised away from the substrate. For instance, electronic assemblies are commonly sealed with conformal coatings. Excessive amounts of the conformal coating material may gather or may form air bubbles under the package if it is raised away from the substrate. This can result in undesirable thermodynamic effects causing movement of the package as the impurities under the package expand and contract due to temperature changes. Such physical instability is especially troublesome in applications requiring tight dimensional

tolerances. For example, an optical fiber interface package--as disclosed in the present application--is one such situation in which tight dimensional tolerances are often required. See Figures 1 through 6.

The present invention prevents unwanted solder flow from short circuiting the leads, while avoiding the aforementioned problems of the existing soldering methods. The present invention achieves this object by providing a level difference along the base of the package proximate the points where the leads are soldered to the substrate. The level difference provides clearance between the leads and the package sufficient to avoid the capillary flow of solder which causes short circuiting. The level difference of the present invention allows the package bottom to rest on the substrate, thus ensuring a level, stable fit. Having the package bottom rest on or near the substrate also avoids air pockets or impurities significant enough to cause problems from accruing beneath the package. Another embodiment of the present inventions avoids the solder flow problem by providing pins with a thick portion at the top, and a thinner portion at the bottom (open) end. See Figures 4 through 6. These later embodiments of the present invention are useful in situations where it is not critical that the bottom of the package rests on the substrate.

Hirata '051 discloses a pin grid array formed with protuberances to ease in handling of the part and to simplify machining. Hirata '051 is said to be primarily concerned with preventing erroneous operations and breakdown *after the device is mounted*. This appears to be the purpose of the eight rows of crosshatched protuberances disclosed by Hirata '051. See Figure 1, protruding part 4. Hirata '051 incidentally discloses a protuberance 12

between each of the dual rows of pins 3 (Figure 1). The protuberance 12 appears to keep the entire pin grid array assembly raised above a substrate to which one might affix it. Hirata '051 neither recognizes nor addresses the problem of capillary attraction as it pertains to soldering.

Hirata '051 differs considerably from the present invention not only in the problem being addressed, but also in the manner of solving that problem. Hirata '051 concerns a pin grid array and appears to be directed towards preventing the problem of unwanted conductive material from coming in contact with the top of the array *after it has been mounted*. Hirata '051 neither recognizes nor solves the problem of trying to prevent solder short circuiting while maintaining the structural integrity and dimensional tolerances of a semiconductor device. This problem is recognized and solved by the present invention.

Hirata '051 also has stark structural differences from the present invention because of the different manner in which it goes about solving its stated problem. The Office Action characterizes protuberances 12 of Hirata '051 as providing the "level difference" feature of claim 1. It is not proper to construe protuberances 12 to be the same as the level difference feature of the claimed invention, for several reasons. First, the protuberance 12 of Hirata '051 does not result in a "level difference between said package and the plurality of leads," as recited in claim 1. Instead, protuberance 12 merely raises the entire pin grid array away from the substrate.

The Hirata '051 device with the entire pin grid array held aloft from the substrate still encounters the problems of the prior art still. Namely, the Hirata '051 device would

take up more space because of its elevated configuration. The present invention avoids this problem because it is not required to be elevated. Also, a raised configuration, such as the one disclosed by Hirata '051, weakens the connecting strength between the package and the substrate because of the relatively longer leads connecting the package and substrate. The present invention does not suffer from this deficiency. Moreover, the Hirata '051 device held aloft by protuberances 12 is subject to having impurities accrue beneath the pin array body. The present invention avoids this significant problem as well.

A further difference between the present invention and the Hirata '051 device is that claim 1 recites "a plurality of leads provided on sides of the package." Hirata '051 discloses only bottom-mount pins. Such a device with bottom mount pins is much more difficult to pick-and-place during assembly than a package with side mount pins as disclosed in the present invention. Additionally, there is no motivation in Hirata '051 to provide pins on the side of the package. In fact, Hirata '051 teaches away from moving the dual rows of pins to the side surface since such a modification would destroy Hirata '051's purpose of providing a high density pin array.

The Office Action further contends that, despite the failure of Hirata '051 to disclose optical elements, it would have been obvious to replace conventional elements with optical elements. Applicants respectfully disagree with this contention. As is commonly known, optical elements are physical devices through which light passes to convey signals. Precise alignment and tight dimensional tolerances are generally important for such optical elements, especially at interface points as disclosed in the present invention. Thus, it

would not have been obvious to substitute an optical element in an application merely sufficient for an ordinary element.

Therefore, Hirata '051 neither teaches nor suggests the features of claim 1, for at least these reasons. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 1, and claim 9 depending therefrom.

The Office Action rejects claim 2 under 35 U.S.C. §103(a) over Japanese Patent 1-39051 (Hirata '051), in view of Japanese Patent 63-174344 (Hirata '344), and further in view of Japanese Patent 4-199556 (Iwanade). Applicants respectfully traverse this rejection. [Note: An apparent typo in the Office Action refers to Japanese Patent 63-174344 as 63-174395 and Hirata '395. Hereinafter, this response refers to Hirata '344.]

Applicants respectfully submit that Hirata '051 suffers from the deficiencies discussed above, regarding claims 1 and 9. For at least the following reasons, Hirata '344 and Iwanade fail to overcome these deficiencies.

Hirata '344 is concerned with fastening a pin grid array to a mother board in two different manners. Namely, Hirata '344 discloses fastening the pin grid array either by inserting pins through the mother board and soldering them, or by having the pin grid array lying on the mother board with the pins facing up and fastening the back of the pin grid array to the mother board.

Iwanade concerns a pin grid array which has two different lengths of pins arranged in alternating fashion. The longer length pins are inserted through holes of the circuit

board and soldered on each side of the circuit board. The shorter length pins are soldered only on the top of the circuit board.

Neither Hirata '344 nor Iwanade overcome the deficiencies of Hirata '051, as discussed above regarding claim 1. In particular, the combination of Hirata '051, in view of Hirata '344, and further in view of Iwanade, fails to disclose "level difference between said package and the plurality of leads." The hypothetical combination of these three patents proposed in the Office Action would seem to suffer from the drawbacks of the prior art. Namely, a device somehow fashioned from the combination of these three patents would require more physical space, would suffer from weakened connecting strength, and would be subject to having impurities accrue beneath the semiconductor device.

Therefore, the combination of Hirata '051, in view of Hirata '344, and further in view of Iwanade, neither teaches nor suggest the features of claim 2, for at least these reasons. Accordingly, Applicants respectfully request withdrawal of this rejection.

The Office Action rejects claim 3 under 35 U.S.C. §103(a) over Hirata '051 in view of Hirata '344. Applicants respectfully traverse this rejection.

As discussed above, Applicants respectfully submit that neither Hirata '051 nor Hirata '344 disclose "level difference between said package and the plurality of leads" recited in claim 3. Therefore, Hirata '051 in view of Hirata '344 neither teach nor suggest the features of claim 3, for at least these reasons. Accordingly, Applicants respectfully request withdrawal of this rejection.

The Office Action rejects claim 4 under 35 U.S.C. §103(a) over Hirata '051, in view of Applicants' Figure 7C. Applicants respectfully traverse this rejection.

As discussed above, Hirata '051 does not disclose the "level difference" feature recited in claim 4. Applicants' Figure 7C does not disclose this feature either. Therefore, the combination of Hirata '051 in view of Applicants' Figure 7C does not teach the features of claim 4. Accordingly, Applicants respectfully request withdrawal of this rejection.

The Office Action rejects claims 5, 6 and 10 under 35 U.S.C. §103(a) over U.S. Patent 5,398,165 (Niinou), in view of Japanese Patent 4-199556 (Iwanade). Applicants respectfully traverse this rejection.

Niinou discloses an electronic circuit component and method of mounting which appears to be aimed at reducing the vibration of the component. To achieve this, Niinou discloses a tapered portion below a shank on each pin. The shank of the pin rests upon the top of the hole of the circuit board, ensuring uniform insertion of the pins and reducing component vibration. The key to Niinou's device is understood to be the tapered portion of the pin, which appears to prevent lateral vibration of the electronic circuit component. Niinou neither recognizes nor addresses the problem of short circuits due to improper solder flow.

The Iwanade patent, as discussed above, discloses a pin grid array with alternating pins of two different lengths. The longer length pins extend through a circuit board and are soldered in place within the holes of the circuit board. The shorter length pins rest on top

of the circuit board and are soldered only to the top of the circuit board. Iwanade neither recognizes nor addresses the problem of short circuits due to improper solder flow.

By contrast to the disclosure of the Iwanade and Niinou patents, independent claim 5 recites that "a shape of said leads provides a level difference" and also recites "said level difference serves to prevent the short-circuiting between the leads." Neither Iwanade nor Niinou disclose such a level difference or even recognize the type of capillary action which leads to solder short circuiting. Therefore, the combination of these two patents fails to disclose the aforementioned feature of claim 5.

A further difference is that claim 5 recites "a plurality of leads provided on sides of the package." Both Iwanade and Niinou disclose in the drawings only semiconductor devices with bottom-mount pin configurations and thus suffer from different problems due to this basic difference construction. Such devices with bottom mount pins are much more difficult to pick-and-place during assembly than are packages with side mount pins as disclosed in the present invention.

Therefore, for at least these reasons the combination of Iwanade and Niinou does not disclose the features of claim 5. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 5, and claims 6 and 10 depending therefrom.

The Office Action rejects claim 7 under 35 U.S.C. §103(a) over U.S. Patent 5,398,165 (Niinou), in view of Japanese Patent 4-199556 (Iwanade). Claim 7 has been amended and now recite "a shape of said leads provides a level difference" and "wherein said level difference serves to prevent the short-circuiting between the leads adjacent to

each other." In addition, the hypothetical combination of these two patents fails to disclose "a plurality of leads provided on sides of the package," as recited in claim 7. Therefore, the features of claim 7 are neither taught nor suggested by Niinou in view of Iwanade. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 7.

The Office Action rejects claim 8 under 35 U.S.C. §103(a) over U.S. Patent 5,398,165 (Niinou), in view of Applicants' Figure 7C. Applicants respectfully traverse this rejection.

As discussed above, Niinou appears to disclose an electronic circuit component and method of mounting intended to reduce the vibration of the component. To reduce vibration, Niinou discloses a tapered portion below a shank upon which the pin rests. The key to Niinou's device seems to be the tapered portion of the pin, intended to prevent lateral vibration of the electronic circuit component.

Niinou fails to disclose that "a shape of said leads provides a level difference" and "wherein said level difference provides different mechanical strengths permitting each of said leads to be bent proximate said package" as recited in claim 8. In fact, Niinou appears to neither recognize or appreciate this feature of claim 8. Likewise, this feature is not disclosed by Applicants' Figure 7C, either.

Therefore, the combination of Niinou and Applicants' Figure 7C teach the features of claim 8. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 8.

While other distinctions exist in the claims, they will not be belabored for the sake of brevity and in light of the differences mentioned above.

In light of the foregoing, Applicants have addressed all issues raised in the Office Action and respectfully submit that the above-captioned application is in condition for allowance. Accordingly, Applicants respectfully request reconsideration and allowance. The Examiner is invited to contact the undersigned at the number listed below, if there are any remaining concerns.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: Scott Charles Richardson

Scott C. Richardson
Registration No. 43,436

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

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